IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (*Currently Amended*): A method of forming device isolation structures in an embedded semiconductor device comprising ~~the steps of~~:

providing a semiconductor substrate having a first area for a power device in which a first type impurity ions are implanted and a second area for a logic device;

forming a first device isolation region through partial oxidation in the first area;

forming a first type well with deep junction by diffusing the ions in the first area during the same partial oxidation process;

forming a second device isolation region with a trench in the second area of the semiconductor substrate;

forming a first type well with shallow junction in peripheral regions of the second device isolation structure and a region between the first device isolation structure and the second device isolation structure;

forming a second type well with shallow junction in peripheral regions of the first device isolation structure and a region of the second device isolation structure; and

defining first and second type active regions on the semiconductor substrate.

2. (*Cancelled*).

3. (*Original*) The method as defined by claim 1, wherein the first type well is an n-type well and the second type well is a p-type well.

4. (*New*) A method of forming device isolation structures in an embedded semiconductor device comprising:

providing a semiconductor substrate having a first area for a power device in which a first type impurity ions are implanted and a second area for a logic device;

forming a first device isolation region through partial oxidation in the first area;

forming a first type well with deep junction by diffusing the ions in the first area;

forming a second device isolation region with a trench in the second area of the semiconductor substrate;

forming a first type well with shallow junction in peripheral regions of the second device isolation structure and a region between the first device isolation structure and the second device isolation structure;

forming a second type well with shallow junction in peripheral regions of the first device isolation structure and an entire region of the second device isolation structure between the first type well with shallow junction; and

defining first and second type active regions on the semiconductor substrate.

5. (*New*) The method as defined by claim 4, wherein the diffusion of ions is simultaneously conducted when the partial oxidation is performed.

6. (*New*) The method as defined by claim 4, wherein the first type well is an n-type well and the second type well is a p-type well.

7. (*New*) A method of forming device isolation structures in an embedded semiconductor device comprising:

providing a semiconductor substrate having a first area for a power device in which a first type impurity ions are implanted and a second area for a logic device;

forming a first device isolation region through partial oxidation in the first area;

forming a first type well with deep junction by diffusing the ions in the first area;

forming a second device isolation region with a trench in the second area of the semiconductor substrate;

forming a first type well with shallow junction in peripheral regions of the second device isolation structure and a region between the first device isolation structure and the second device isolation structure with a first photoresist pattern, the first device isolation and the second device isolation having a first mask;

forming a second type well with shallow junction in peripheral regions of the first device isolation structure and a region of the second device isolation structure with a second photoresist pattern, the first device isolation and the second device isolation having a second mask; and

defining first and second type active regions on the semiconductor substrate.

8. (*New*) The method as defined by claim 7, wherein the diffusion of ions is simultaneously conducted when the partial oxidation is performed.

9. (*New*) The method as defined by claim 8, wherein the first type well is an n-type well and the second type well is a p-type well.